REMARKS

Applicant appreciates the detailed examination evidenced by the Official Action mailed April 20, 2006 (hereinafter "the Official Action"). Applicant also appreciates the allowance of Claims 29-37 and the indication that Claims 15-19 would be allowable if rewritten as suggested by the Examiner. *Official Action, pages 4-5.*

In response, Applicant has amended the application as follows:

1. Claim 15 has been amended to include the recitations of Claim 14, thereby placing Claims 15-19 in condition for allowance.
2. Claim 25 has been amended to adjust the dependency thereof to Claim 20 as suggested by the Examiner.
3. Claim 20 has been amended to recite a combination of means elements as suggested by the Examiner.

In view of the above amendments and the following remarks, Applicant respectfully submits that all pending claims are in condition for allowance for at least the reasons described herein.

The Rejections Under 35 U.S.C. § 112 Have Been Overcome By Amendment.

Claims 14-19 and 25 stand rejected under 35 U.S.C. § 112, second paragraph. *Official Action, page 2.* In particular, the Official Action objected to the recitation of "modifying access to the DFS cache memory" as recited in original Claim 14. In response, Applicant has cancelled Claim 14 and has incorporated the recitations thereof into allowable Claim 15. Applicant also notes that amended Claim 15 recites, in-part, that "modifying" comprises:

> accessing the DFS main cache memory without accessing the DFS line buffer cache memory when the DFS cache memory is operating according to the high frequency DFS clock; and
>
> accessing the DFS line buffer cache memory responsive to a miss on accessing the DFS main cache memory when the DFS cache memory is operating according to the low frequency DFS clock,

that further clarifies the recitation of "modifying" to ensure that these claims fully comply with section 112. According, Claims 15-19 are condition for allowance, which is respectfully requested in due course.

With regard to the rejection of Claim 25, Applicant has amended this claim to change the dependency thereof from Claim 19 to Claim 20 as suggested by the Examiner. Accordingly, the rejection of Claim 25 under Section 112 has been overcome by amendment and is respectfully requested to be withdrawn.

Claims 20-22 also stand rejected under 35 U.S.C. § 112, first paragraph. *Official Action, page 3.* In particular, the Official Action has characterized this claim as a "single means claim." In response, Applicant has amended independent Claim 20 to recite in part:

> means for accessing a DFS cache memory during an active time interval in a single low frequency DFS clock cycle; and
> means for accessing the DFS cache memory during an idle time, after the active time interval, in the single low frequency DFS clock cycle.

As demonstrated by the above recitations of amended Claim 20, this claim now recites a combination of means elements including a "means for accessing a DFS cache memory during an active time interval . . . and means for accessing a DFS cache memory during an idle time . . ." Accordingly, the rejections of Claim 20-22 have been overcome by amendment and are respectfully requested to be withdrawn.

The Pending Claims Are Patentable Over Shirotori.

Claims 1-14 and 20-28 stand rejected under 35 U.S.C. § 102 over U.S. Patent No. 5,920,888 to Shirotori et al. ("Shirotori"). *Official Action, page 3.* Applicant respectfully traverses the rejection of these claims as Shirotori does not disclose the specific recitations of the pending claims including, for example, independent Claim 1, which recites, in part:

> accessing a DFS cache memory **during an idle time in a single low frequency DFS clock cycle**.

Independent Claim 26 includes similar recitations.

As demonstrated by the above-highlighted recitations of independent Claim 1, Shirotori does not disclose accessing a DFS cache memory **during an idle time in a single low frequency DFS clock cycle**. To the contrary, the portions cited in support of the rejection show that Shirotori **accesses the cache during an active portion of a single low frequency DFS clock cycle, not an idle time**. For example, Figure 8 of

Shirotori shows a tag read followed by a data read only during an active portion of a single low frequency DFS clock cycle (*i.e.*, the high-going portion of the clock pulse in Figure 8).

In contrast to Shirotori, in some embodiments according to the invention as illustrated, for example, in Figure 2 of the Application, during a single low frequency DFS clock cycle A, an access to the line buffer cache is performed during a first portion of the single low frequency DFS clock cycle and an access to the main cache memory is performed during the idle time of the same single low frequency DFS clock cycle.

Moreover, the passages of Shirotori cited by the Official Action in support of the rejection also indicate Shirotori avoids using the latter portion of the single low frequency DFS clock cycle shown in Figure 8:

> (a) FIG. 8 shows the low-speed mode with the frequency of the reference clock signal CLK being low as shown in FIG. 5C. The pulse width of the reference pulse signal PLS is compared with the half-period of the reference clock signal CLK. It is checked to see if the reference clock signal CLK rises while the reference pulse signal PLS is high. If it is so, the high-speed mode is started, and if not so, the low-speed mode of low power consumption is started. An interval between a fall of the reference pulse signal PLS and a rise of the next period of the reference clock signal CLK is detected to generate the signal A. **A read operation of the data memories 2 is delayed by a high-level interval of the signal A.** If the delayed start of reading the data memories 2 is before the completion of checking tags as shown in FIG. 8, only a hit one of the data memories 2 is read to realize the low-speed mode with minimum power dissipation. *Shirotori, Column 6, lines 21-26.* (emphasis added)

As shown by the above-cited passage of Shirotori, the discussion therein indicates an intention to actually delay a subsequent access to the cache memory to avoid an access during the same single low frequency DFS clock cycle and, rather, to perform the access in a subsequent low frequency DFS clock cycle. Accordingly, Shirotori does not disclose the recitations of independent Claim 1 for at least the reasons described above. Furthermore, Claims 2-9 are patentable at least per the patentability of independent Claim 1 and Claims 27 and 28 are patentable at least per the patentability of independent Claim 26.

Shirotori also does not disclose the recitations of independent Claim 10, which recites, in part:

> accessing a DFS filter cache memory at a first time in a single low frequency DFS clock cycle; and
> accessing a DFS cache memory at a second time in the single low frequency DFS clock cycle responsive to a miss on accessing the DFS filter cache memory.

As described above in reference to independent Claim 1, Shirotori does not disclose accessing a DFS cache memory **during an idle time**. In addition, Shirotori also does not disclose, for example, accessing a DFS filter cache memory at a first time in a single low frequency DFS clock cycle and accessing a DFS cache memory at a second time in the single low frequency DFS clock cycle **responsive to a miss on accessing the DFS filter cache memory**.

The only other access shown in Shirotori during a single low frequency DFS clock cycle is the data read during the initial portion of the single clock cycle CLK shown in Figure 8.[1] However, as demonstrated by the above-cited passage of Shirotori, the read of data in the single low frequency DFS clock cycle of Figure 8 is only done with a hit occurs on the tag read:

> If the delayed start of reading the data memories 2 is before the completion of checking tags as shown in FIG. 8, **only a hit one of the data memories 2 is read to realize the low-speed mode with minimum power dissipation**. *Shirotori, Column 6, lines 33-36.* (emphasis added)

As shown by the above-cited passage of Shirotori, the only other access performed during a single low-frequency DFS clock cycle in Shirotori is done responsive to a hit, not a miss. Furthermore, as described above, the read of the data during the single low frequency DFS clock cycle shown in Figure 8 of Shirotori is also not performed during the idle time. Accordingly, independent Claim 10 is patentable over Shirotori for at least the reasons described herein. Furthermore, dependent Claims 11-13 are patentable at least per the patentability of independent Claim 10.

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[1] Applicant acknowledges that Figures 9 and 10 appear to show other types of accesses, but these do not disclose access during a single low frequency DFS clock cycle as Figure 9 shows a medium speed access and Figure 10 shows a high speed access. *Shirotori, col. 6, lines 37-63.*

Shirotori also does not disclose the recitations of amended Claim 20 which recites in part:

> means for accessing a DFS cache memory **during an active time interval in a single low frequency DFS clock cycle**; and
>
> means for accessing the DFS cache memory **during an idle time, after the active time interval, in the single low frequency DFS clock cycle**.

As demonstrated by the above-highlighted recitations of independent Claim 20, Shirotori does not disclose, at least, "means for accessing a DFS cache memory during an active time interval in a single low frequency DFS clock cycle" and "means for accessing the DFS cache memory during an idle time after the active time interval . . ." As described above in reference to independent Claims 1 and 11, the discussion in Shirotori on low frequency access shows access **only during an active time interval** (*i.e.*, initial time interval) of a single low frequency DFS clock cycle and, therefore, does not disclose accessing. . . "during an active time interval in the single low frequency DFS clock cycle and accessing during an idle time after the active time interval . . ." Accordingly, independent Claim 20 is patentable over Shirotori for at least these reasons. Furthermore, dependent Claims 21-25 are patentable at least per the patentability of amended independent Claim 20.

CONCLUSION

Applicant has provided amendments and remarks herein illustrating that the pending claims are patentable over Shirotori for at least the reasons described herein. Accordingly, Applicant respectfully requests the withdrawal of all rejections and the allowance of all claims in due course. If any informal matters arise, the Examiner is encouraged to contact the undersigned by telephone at (919) 854-1400.

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